being part of said metallic layer.

5. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having at least one DRAM region and one logic region;

a signal interconnection layer in said logic region; and

a metallic layer in said DRAM region and said logic region and located on one side of said signal interconnection layer, with respect to said semiconductor substrate, as a shielding layer in said logic region.

6. (Twice Amended) The semiconductor device according to claim 5, wherein said metallic layer is a gate electrode layer in said DRAM region.

7. (Twice Amended) The semiconductor device according to claim 5, wherein said metallic layer is a bit line layer in said DRAM region.

8. (Twice Amended) The semiconductor device according to claim 5, comprising stacked capacitor in said DRAM region and including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, said upper capacitor electrode layer in said DRAM region being part of said metallic layer.

10. (Twice Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a metallic layer as a shielding layer in said logic region and in said DRAM region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

11. (Twice Amended) The method according to claim 10, wherein said metallic layer is a bit line layer in said DRAM region.

12. (Twice Amended) The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer is part of said metallic layer.

B6 C1 14. (Twice Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a first metallic layer as a first shielding layer in said logic region and in said DRAM region;

forming a signal interconnection layer in said logic region opposite said first shielding layer; and

forming a second metallic layer as a second shielding layer opposite said signal interconnection layer in said logic region and in said DRAM region.

B7 C1 15. (Amended) The method according to claim 14, wherein one of said first and second metallic layers is a gate electrode layer in said DRAM region.

16. (Amended) The method according to claim 14, wherein one of said first and second metallic layers is a bit line layer in said DRAM region.

B8 C1 17. (Twice Amended) The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer in said DRAM region is part of said second metallic layer.

18. (Twice Amended) The method according to claim 14, further comprising fixing potential of one of said first and second shielding layers.